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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/009,826	03/19/2002	Hideyuki Matsuoka	XA-9594	6166

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EXAMINER	
NGUYEN, CUONG QUANG	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 03/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/009,826	MATSUOKA ET AL.	
	Examiner	Art Unit	
	Cuong Q Nguyen	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) *31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,15-30 and 32-35* is/are rejected.

7)☒ Claim(s) *14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *030202*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

1. Applicant's election of Group I, claims 1-30 and 32-35 on 12-08-03 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation "teach the conductive layer of the memory device is a conductive layer connected to a gate electrode of an insulated gate FET in the peripheral circuit" in claim 14 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 4-13, 17-23, 27, 28, 30, 33, 34 and 35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation "the potential can be applied to the insulating layer" in claim 1 makes the claim indefinite because the term "can be" is a non-certain term.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4, 24, 25, and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Johnson et al (US 6,034,882).

Regarding claims 1, 4, Johnson et al. disclose a semiconductor memory device comprosing: a semiconductor substrate (col.5 line 39-41 and col.13 lines 27-35); a memory cell array disposed on the semiconductor substrate having plural memory cells, word lines and datalines (bit lines) (col.7 lines 31-36); and a peripheral circuit formed on the semiconductor substrate; wherein the memory cell has a multi-layer of a conductive layer (48, 480), an insulating layer (42, 420), N-type plysilicon layers (41, 43, 410, 430) and a P-type polysilicon layer (40, 400); and a poltential being applied to the insulating

layer that enables the movement of carriers by way of the multi-layer. See Johnson et al.'s Fig.4(b) and Fig.6(a).

Regarding claim 2, Johnson et al. teaches that the multi-layer of the memory cell has bistable characteristics for the resistance value. Col.12 lines 20-29.

Regarding claims 24, 25, as shown in Johnson et al.'s Fig.10(a) and Fig.10(b), the plural data lines arranged so as to intersect the plural word lines in a planer arrangement; plural memory cells which are disposed each at a desired intersection bwteen the plural word lines and the plural data lines and each connected to the corresponding word line and corresponding data lines; a common data line disposed in common with the plural data lines; and plural signal transmission means having a swching fuction (switching transistors) for connecting the common data line to the plural data lines respectively.

Regarding claim 32, it is noted that Johnson et al.'s device has a structure identical as claimed device. So, it is inherent that Johnson et al.'s device would have been functioning as claimed device such that when a potential is applied to the insulating layer capable of moving carriers by way of the multi-layer has a hysteresis characteristic relative to applied voltage.

Claim 29 is rejected under 35 U.S.C. 102(b) as being anticipated by Kroger et al. (US 3,979,613).

Kroger et al. Discloses a semiconductor device wherein a bistable diode is configured to have a region (62) included in a semiconductor substrate (3). Fig.19.

Claim 3, 15, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Komori et al. (US 5,904,518).

Regarding claim 3, Komori et al. discloses a semiconductor memory device comprising: a semiconductor substrate (1); a memory array formed on the semiconductor substrate; word lines and data lines for selecting the memory cells; a peripheral circuit formed on the semiconductor substrate which is constituted with plural insulated gate FETs on the peripheral of the memory cell array; wherein the memory cell has a multi-layer of a conductive layer (9, 7); an insulating layer (6) that enables the tunnel effect and plural semiconductor layers (P-type layer 13 and N-type layer 11, 12, 14, 17) containing impurities are present in the semiconductor substrate. See Komori et al.'s Fig.1.

Regarding claim 15, as shown in Komori et al.'s Fig.1, the muti-layer contains N-type polysilicon layer (7, 9).

Regarding claim 16, as shown in Komori et al.'s Fig.1, the insulating layer (6) of the memory cell is an insulating layer connected with an insulating layer (8) of an insulated gate FET in the peripheral circuit.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Komori et al.

Komori et al. teaches all the limitations of claims 3, 15 and 16 as shown above. However, Komori does not explicitly teach that a common data line disposed in common with the plural data lines and plural signal tranmission means having a switching function for connecting the common data line respectivitly.

It would have been obvious to one of ordinary skill in the art to form the Komori et al.'s memory device having above arrangement as claimed because such arrangement is conventional and well known in the art.

Allowable Subject Matter

6. Claim 14 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is an examiner's statement of reasons for allowance: Komori et al. appears to be the closest prior art reference. However, this reference fails to teach the conductive layer of the memory device is a conductive layer connected to a gate electrode of an insulated gate FET in the peripheral circuit. Prior art of record fails to teach or suggest to incorporate these limitations into Komori et al. to arrive at the claimed device.

Conclusion

8. Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 872-9306. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

9. Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to CUONG Q NGUYEN whose telephone number is (571) 272-1661. The Examiner is in the Office generally between the hours of 6:30 AM to 5:00 PM (Eastern Standard Time) Monday through Thursday.

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Eddie Lee who can be reached on (571) 272-1732.

11. Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center Receptionists whose telephone number is 308-0956.

Cuong Nguyen

Primary examiner

3/8/04